Amendment of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An apparatus for providing failsafe detection for a differential receiver that produces a bus activity indicator signal when receiving a differential data signal of sufficient amplitude to transition through a first predetermined receiver threshold, said apparatus comprising:

a window comparator having an input ~~for coupling~~ coupled to said differential receiver and operable to activate a failsafe signal when a ~~low differential voltage condition transition~~ transition below a second predetermined threshold occurs on said differential receiver[[;]] , said second predetermined threshold being less than said first predetermined threshold;

a timer coupled to said window comparator and having an input to receive said bus activity indicator signal and said failsafe signal, said timer operable for deactivating a timeout signal in response to each activation of said bus activity indicator signal and said failsafe signal, said timer further for activating said timeout signal if a predetermined period of time elapses since a most recent deactivation of said timeout signal; and

a failsafe indicator gate coupled to said timer and said window comparator to receive said timeout signal and said failsafe signal, and having an output to set a flag when said failsafe signal and said timeout signal are both active.

2. (original) The apparatus of Claim 1, wherein said failsafe indicator gate comprises an OR gate.

3. (currently amended) The apparatus of Claim 1, wherein said window comparator further comprises:

first and second comparators configured to compare said differential data signal with respective first and second references, wherein said first and second references are at said second threshold and represent a failsafe threshold; and

a logic gate coupled to said comparators to receive outputs from said comparators.

4. (original) The apparatus of Claim 3, wherein said timer includes an exclusive OR gate which receives said bus activity indicator signal and failsafe signal as inputs, and wherein an output of said exclusive OR deactivates said timeout signal.

5. (original) The apparatus of Claim 1, further comprising a delay device coupled between said window comparator and said failsafe indicator gate to delay arrival of said failsafe signal at said failsafe indicator gate for a delay time period.

6. (original) The apparatus of Claim 5, wherein said delay time period exceeds an amount of time required for said timer to deactivate said timeout signal.

7. (original) The apparatus of Claim 6, wherein said delay device comprises an RC circuit.

8. (currently amended) A system for providing failsafe detection in a differential receiver network, said system comprising:

a differential input device configured to provide a timer reset signal upon receiving a differential data signal of sufficient amplitude to transition through a predetermined receive threshold;

a fault detection device coupled to said differential input device and configured to provide an indicator signal when said differential data signal transitions into a fault threshold region[[;]], said fault threshold being less than said receive threshold;

a resettable timer coupled to said differential input device and said fault detection device and configured to provide a timeout signal upon expiration of a predetermined amount of time after receiving either said timer reset signal or said indicator signal; and

a failsafe indicator device [[or]] coupled to said timer and said fault detection device and configured to set a flag when said indicator signal persists following expiration of said amount of time.

9. (original) The system of Claim 8, wherein said failsafe indicator device comprises an OR gate which receives said timeout signal and said indicator signal as inputs.

10. (currently amended) The system of Claim 8, wherein said fault detection device further comprises:

first and second comparators configured to compare said differential data signal with respective first and second references, wherein said first and second references are at said fault threshold and represent a failsafe threshold; and

a logic gate coupled to said comparators to receive outputs from said comparator.

11. (original) The system of Claim 10, wherein said timer includes an exclusive OR gate that receives said timer reset signal and said indicator signal as inputs, and wherein an output of said exclusive OR gate initiates activation of said timeout signal.

12. (original) The system of Claim 8, further comprising a delay device coupled between said fault detection device and said failsafe indicator device to delay arrival of said indicator signal at said failsafe indicator device for a delay time period.

13. (original) The system of Claim 12, wherein said timer is operable for initially deactivating said timeout signal upon receiving either said timer reset signal or said indicator signal, and wherein said delay time period exceeds an amount of time required for said timer to deactivate said timeout signal.

14. (original) The system of Claim 13, wherein said delay device comprises an RC circuit.

15. (currently amended) A method of providing failsafe detection in a differential receiver circuit, said method comprising;

comparing a differential data signal received by said differential receiver circuit to a predetermined receive threshold , said failsafe threshold being less than said receive threshold, and commencing a countdown time period upon detecting a receive threshold transition;

comparing said differential data signal to a predetermined failsafe threshold and commencing a countdown time period upon detecting a failsafe threshold transition; and

setting an indicator flag upon detecting a failsafe threshold transition following expiration of one of the countdown time periods.

16. (original) The method of Claim 15, wherein said setting step includes using an OR gate to set said indicator flag, and including said OR gate receiving indications of both of said threshold transitions.

17. (original) The method of Claim 15, wherein said setting step includes using a first logic gate to set said indicator flag, and including said first logic gate receiving indications of both of said threshold transitions, and wherein said commencing steps include using a second logic gate to commence the countdown time periods, and including said second logic gate receiving indications of both of said threshold transitions.

18. (original) The method of Claim 15, wherein said commencing steps include using an exclusive OR gate to commence the countdown time periods, and including said exclusive OR gate receiving indications of both of said threshold transitions.

19. (original) The method of Claim 15, including providing a failsafe condition indication in response to said first-mentioned detecting step, said second-mentioned detecting step including delaying said failsafe condition indication for a delay period of time.

20. (original) The method of Claim 19, wherein said delay period exceeds an amount of time required for commencement of one of the countdown time periods after detection of the corresponding threshold transition.